Please write clearly in block capitals.

Centre number | | | | | | Candidate number | | | | |

Surname ______________________

Forename(s) ______________________

Candidate signature ______________________
I declare this is my own work.

A-level PHYSICS

Paper 3
Section B Electronics

Time allowed: The total time for both sections of this paper is 2 hours. You are advised to spend approximately 50 minutes on this section.

Materials
For this paper you must have:
- a pencil and a ruler
- a scientific calculator
- a Data and Formulae Booklet
- a protractor.

Instructions
- Use black ink or black ball-point pen.
- Fill in the boxes at the top of this page.
- Answer **all** questions.
- You must answer the questions in the spaces provided. Do not write outside the box around each page or on blank pages.
- If you need extra space for your answer(s), use the lined pages at the end of this book. Write the question number against your answer(s).
- Do all rough work in this book. Cross through any work you do not want to be marked.
- Show all your working.

Information
- The marks for questions are shown in brackets.
- The maximum mark for this paper is 35.
- You are expected to use a scientific calculator where appropriate.
- A Data and Formulae Booklet is provided as a loose insert.

For Examiner's Use	
Question	Mark
1	
2	
3	
4	
5	
TOTAL	

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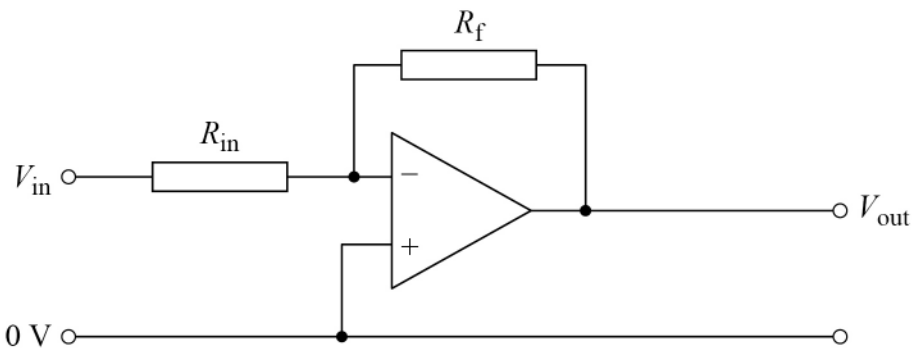
ANSWER IN THE SPACES PROVIDED

Section B

Answer **all** questions in this section.

0 1 **Figure 1** shows a circuit containing an ideal operational amplifier. A signal V_{in} is applied to one of the amplifier inputs.

Figure 1



0 1 . 1 Draw an **X** on the circuit in **Figure 1** to indicate a virtual earth point.

[1 mark]

0 1 . 2 Show that the closed loop voltage gain for the amplifier in **Figure 1** is given by:

$$\frac{R_f}{R_{in}} = -\frac{V_{out}}{V_{in}}$$

State any assumptions made in your answer.

[2 marks]

assumptions ______________________________

____

Question 1 continues on the next page

0 1 . 3 **Figure 2A** shows the input signal V_{in} that is applied to the circuit in **Figure 1**.

Figure 2A

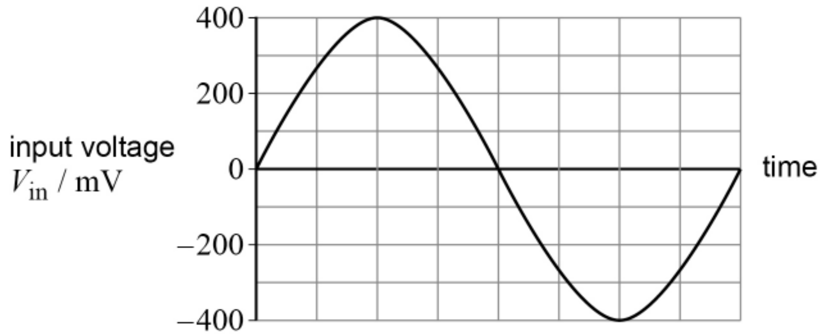
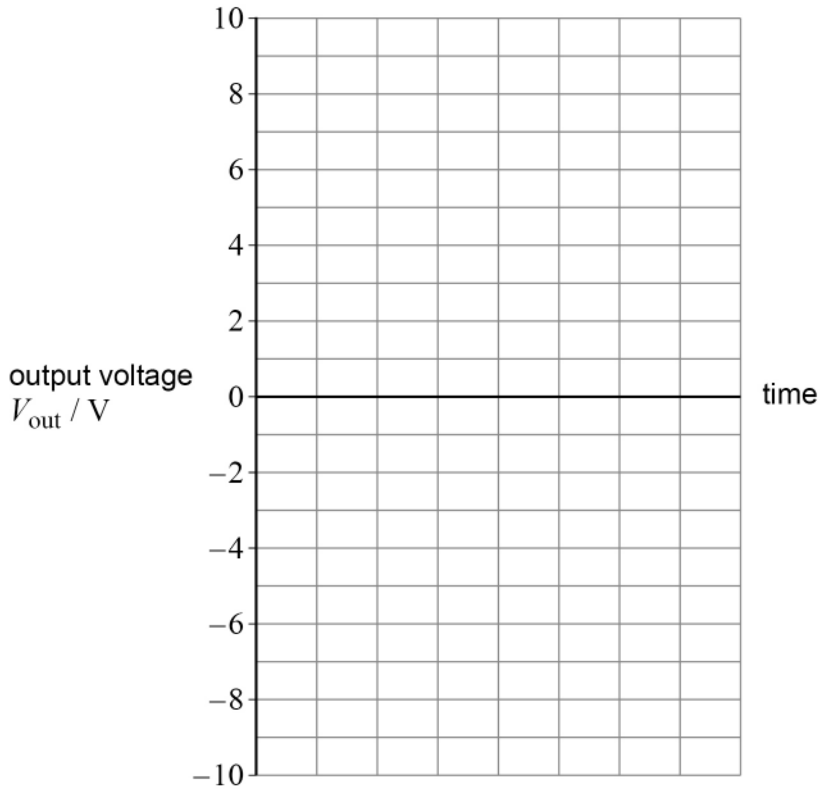


Figure 2B



The circuit in **Figure 1** has a closed loop gain of -20 and has power-supply voltages of $\pm\ 6.0\ \text{V}$.

Draw, on **Figure 2B**, the output waveform from the operational amplifier circuit over the same time interval as that shown on **Figure 2A**.

[2 marks]

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0 1 . 4 A student converts the circuit in **Figure 1** into one that will add two input signals V_1 and V_2.

The new circuit produces an output voltage V_{out} so that:

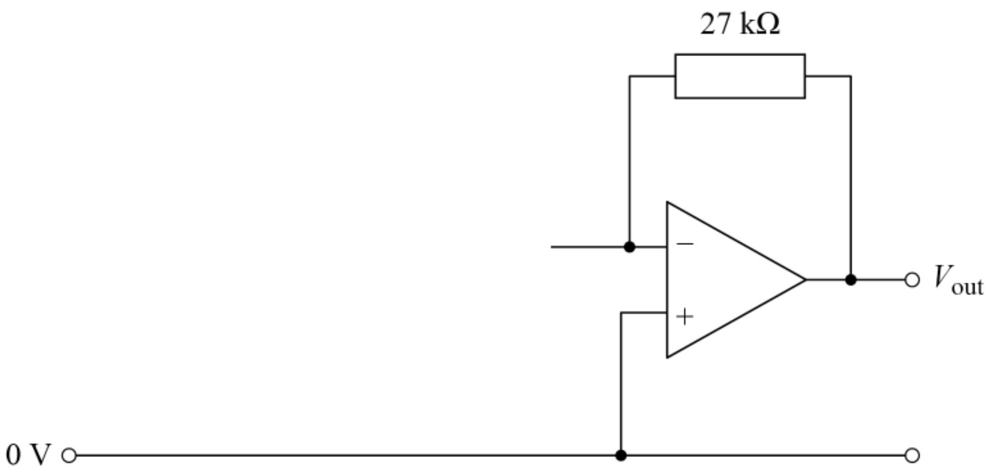
$$V_{\text{out}} = -(1.5V_1 + 0.75V_2)$$

The circuit is to include a $27\ \text{k}\Omega$ feedback resistor.

Complete **Figure 3** to show the circuit that the student constructs.
Annotate your circuit with the values of any additional components.

[3 marks]

Figure 3



8

Turn over for the next question

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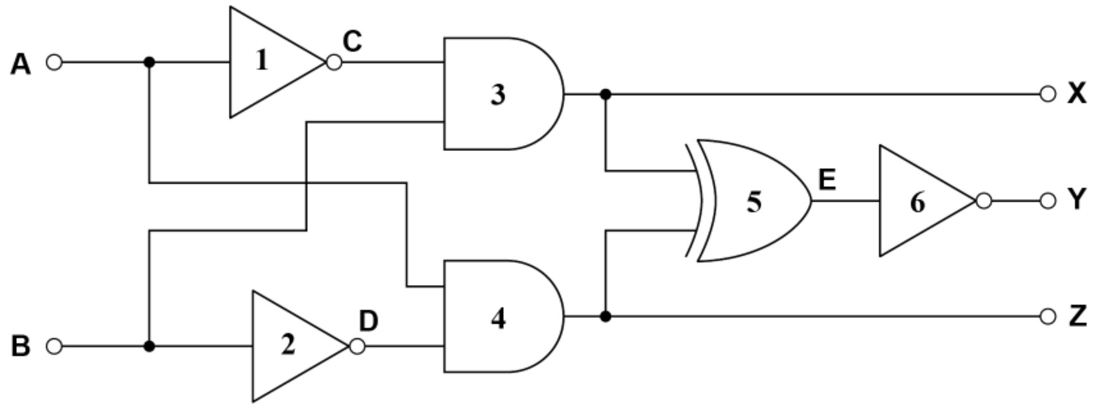
0 2 **Figure 4** shows a logic system made of logic gates labelled **1** to **6**
The logic system has inputs **A** and **B** and outputs **X**, **Y** and **Z**.

Figure 4



0 2 . 1 Write the simplest Boolean algebra expression for output **X** in terms of inputs **A** and **B**.

[2 marks]

X = ____________________

0 2 . 2 State the name of logic gate **5** in **Figure 4**.

[1 mark]

____

0 2 . 3 Complete **Table 1**, the truth table for this logic system.

[2 marks]

Table 1

B	A	C	D	E	X	Y	Z
0	0	1	1	0			
0	1	0	1	1			
1	0	1	0	1			
1	1	0	0	0			

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0 2 . 4 Suggest a single logic gate that can replace the combination of gates **5** and **6** in this system.

[1 mark]

____

0 2 . 5 The logic system in **Figure 4** is designed to indicate which of inputs **A** and **B** has the larger binary value, or whether the values are the same. Each decision is indicated by one of the outputs **X**, **Y** or **Z** becoming a logic 1

Which row identifies the outputs **X**, **Y** and **Z**?
Tick (✓) **one** box.

[1 mark]

X	Y	Z	
A = B	A < B	A > B	☐
A < B	A = B	A > B	☐
A < B	A > B	A = B	☐
A > B	A = B	A < B	☐

7

Turn over for the next question

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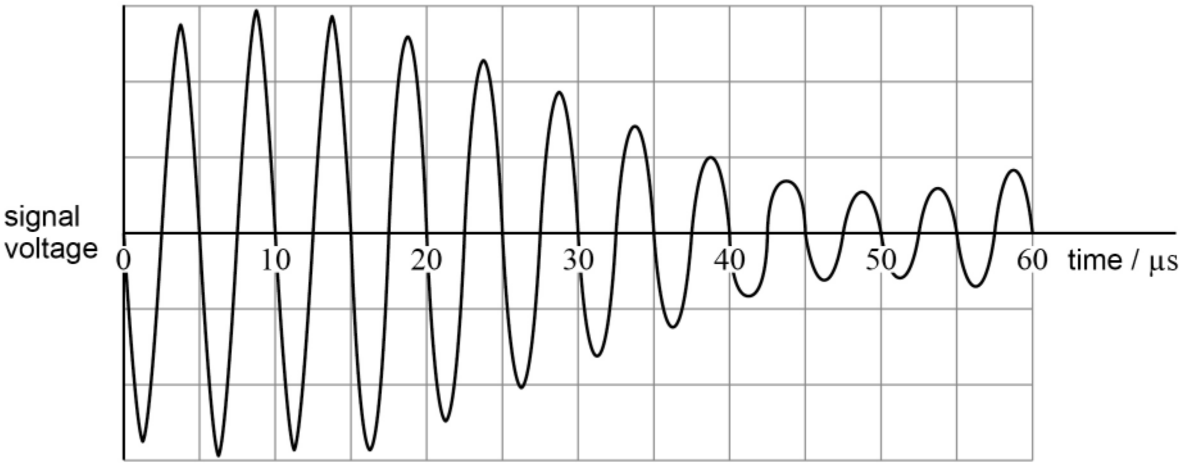
0 3 **Figure 5** shows the output signal from the tuner circuit of a radio receiver.

The radio carrier wave is amplitude modulated by a single-frequency test tone.

Figure 5



0 3 . 1 Determine the frequency, in kHz, of the carrier wave.

[1 mark]

frequency of carrier wave = ______________________ kHz

0 3 . 2 Determine the frequency, in kHz, of the test tone.

[2 marks]

frequency of test tone = ______________________ kHz

0 3 . 3 State **one** advantage of using frequency modulation (FM) rather than amplitude modulation (AM).

[1 mark]

---

0 3 . 4 The frequency range of the FM radio band in the UK is 88 to 108 MHz.

The FM stations are allocated centre frequencies that start at 88.100 MHz and are separated by 200 kHz.

Calculate the maximum number of stations allowed within the range.

[1 mark]

maximum number of stations = ____________________

0 3 . 5 A radio station broadcasting on FM transmits a maximum audio frequency of 15 kHz and has a frequency deviation of ± 75 kHz.

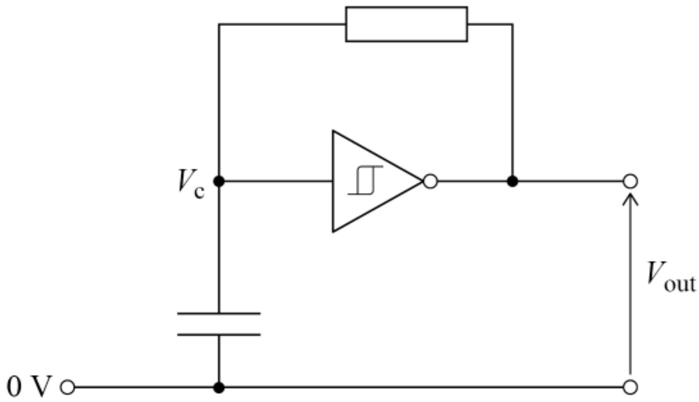
Deduce whether the radio station fits the FM bandwidth allocation in the UK.

[2 marks]

7

0 4 **Figure 6** shows a type of NOT gate called a Schmitt Trigger. This is connected to a capacitor of capacitance C and a resistor of resistance R to make an oscillator circuit. The circuit is used to produce continuous clock pulses.

Figure 6



V_{out} switches HIGH or LOW when the input voltage V_c passes through one of two trigger voltage values.

The output voltage V_{out} switches to:

- LOW when V_c rises and reaches the upper trigger voltage V_U
- HIGH when V_c falls and reaches the lower trigger voltage V_L.

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0 4 . 1 Initially the capacitor is uncharged and V_c is at 0 V.

Explain the sequence of actions of this circuit as the output goes through one full cycle. The first two stages have been done for you.

You should refer to the RC circuit in **Figure 6** and to V_U and V_L in your answer.

[3 marks]

Stage 1: Since V_c is LOW, the output is HIGH.

Stage 2: The capacitor now charges through the resistor, making V_c rise.

Stage 3: ____________________

____

____

Stage 4: ____________________

____

____

Stage 5: ____________________

____

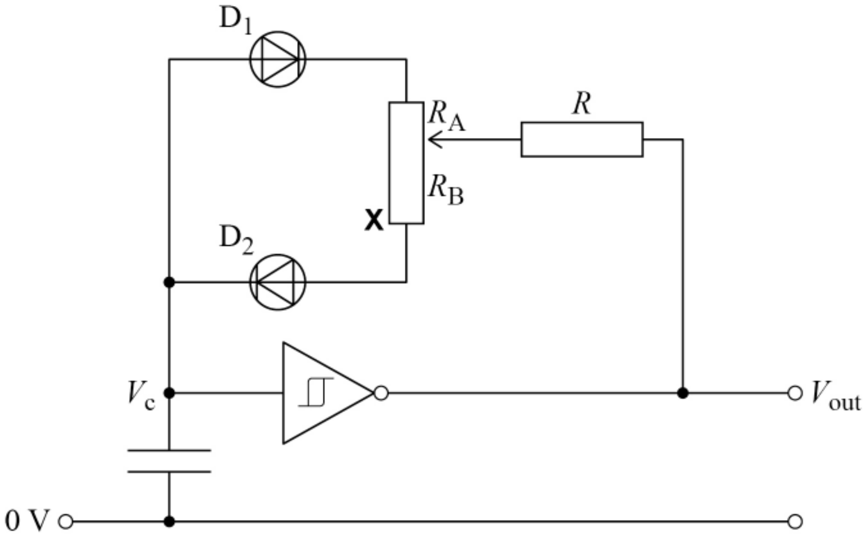
____

Question 4 continues on the next page

0 4 . 2 **Figure 7** shows the oscillator circuit after it has been modified by the addition of:

- two diodes D_1 and D_2
- a potential divider that has a total resistance value of (R_A + R_B).

Figure 7



In this particular circuit:

- the time t_H for the output signal to be HIGH is given by $t_H = 0.7C\,(R + R_B)$
- the time t_L for the output signal to be LOW is given by $t_L = 0.7C\,(R + R_A)$.

The slider of the potential divider is moved towards **X**, as shown in **Figure 7**.

State and explain the effect of this change on:

- the mark-to-space ratio ($t_H : t_L$)
- the pulse rate frequency (PRF).

[4 marks]

mark-to-space ratio ____

____

____

____

____

____

PRF ____

____

____

____

____

____

7

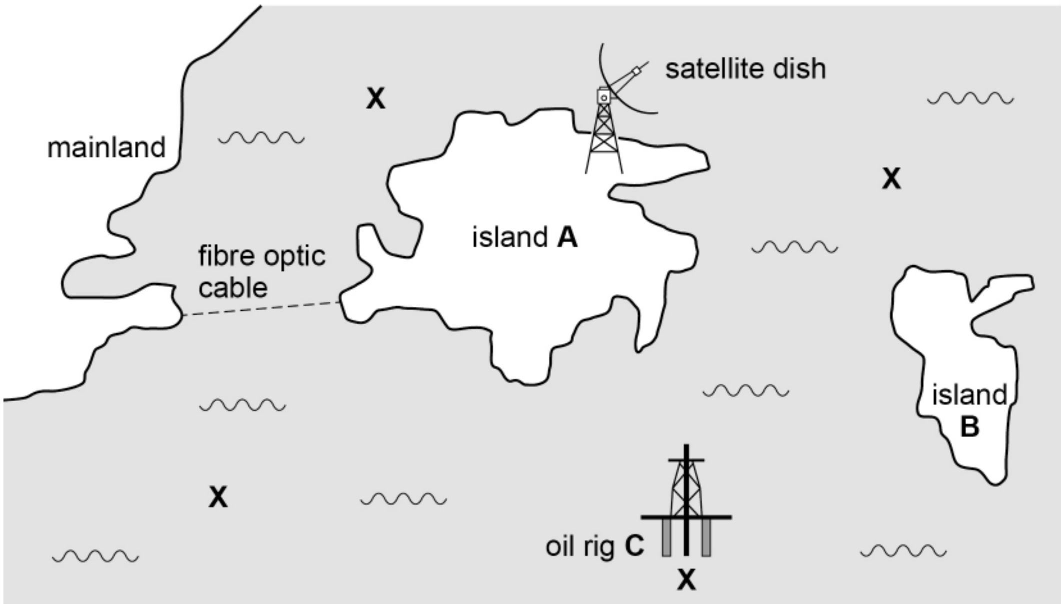
Turn over for the next question

0 5 **Figure 8** shows island **A**, a fully developed island off the mainland coast. The island is connected to the mainland by a fibre optic cable lying along the seabed and it also has a satellite link.

Nobody lives on island **B**, but it is due to be developed as a major holiday resort over the next 5 years.

Moveable oil rig **C** is due to explore the four sites marked '**X**' for oil and gas over a 9-month period.

Figure 8



A communications company has been asked to provide solutions for island **B** which will allow the development to begin immediately and then later to support a fully developed holiday resort.

A communications solution is also required for oil rig **C** during the 9-month exploration period.

Describe appropriate solutions involving fibre optic cabling and satellite communication systems for each of the two clients, island **B** and oil rig **C**.

In your answer you should:

- outline the way each communications system operates
- suggest, with reasons, your choice of system for each solution.

[6 marks]

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6

END OF QUESTIONS

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